Yosi Ben Asher: List of Publications

1.

2. **Y. Ben Asher**, "*The Cartesian Product Problem and Implementing Production Systems on Reconfigurable Meshes*", Parallel Processing Letters, Vol. 5 No. 1, pp. 49-61, 1995.
IF=1.12 (from ResearchGate 2012)

3. **Y. Ben Asher**, D. Gordon and A. Schuster, "*Efficient Self Simulation Algorithms in Reconfigurable Arrays*", Journal of Parallel and Distributed Computing (JPDC), Vol. 30, pp. 1-22, 1995.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

4. **Y. Ben Asher**, A. Schuster and J.F. Sibeyn, "*Load Balancing: A Programmer's Approach or The Impact of Task-Length Parameters on the Load Balancing Performance of Parallel Programs.*", International Journal of High-Speed Computing, Vol. 7, No. 2, pp. 303-325, 1995.
IF=0.15 IF5y=N.A 65/71 computer science, theory&methods Q4.

5. **Y. Ben Asher**, K. Lange, D. Peleg and A. Schuster, "*The Complexity of Reconfiguring Network Models*", Information and Computation, Vol. 21, (1) pp. 41-58, 1995.
IF=0.87 IF5y=0.91 60/105 computer science, theory&methods Q2.

6. **Y. Ben Asher**, G. Rünger, A. Schuster and R. Wilhelm, "*2DT-FP: An FP Based Programming Language for Efficient Parallel Programming of Multiprocessor Networks*", International Journal of Parallel Programming (IJPP), Vol 23, No 5, pp. 389-422, 1995.
IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

7. **Y. Ben Asher** and I. Newman, "*Decision Trees with Boolean Threshold Queries*", Journal of Computer and System Sciences (ICSS), Vol. 51, No. 3, pp. 495-502, 1995.
IF=1.58 IF5y=1.59 14/51 computer science, hardware&architectures Q2.

8. **Y. Ben Asher**, and A. Schuster, "*Low Crosstalk Address Encodings for Optical Message Switching Systems*", Parallel Processing Letters, vol. 6, no. 1, pp. 87-100, Feb. 1996.
IF=1.12 (from ResearchGate 2012)

9. **Y. Ben Asher**, D. Feitelson and L. Rudolph, "*Parc, An extension of* C", Journal of Software practice & Experience, Vol. 26, No. 5, pp. 581-612, 1996.
IF=1.0 IF5y=1.25 76/106 computer science, software engineering Q3.

10. **Y. Ben Asher**, A. Cohen and A. Schuster, "*Tradeoffs Between Size and Time in Reconfigurable Meshes*", Parallel processing letters (PPL), volume 6 number 2, 1996.
IF=1.12 (from ResearchGate 2012)

11. G. Haber and **Y. Ben Asher**, "*On the Usage of simulators to detect inefficiency of parallel programs caused by "bad" schedulings: the SIMPARC approach*", Journal of Systems and Software, Vol. 33, No. 3, pp. 313-333, 1996.
IF=1.42 IF5y=1.76 24/106 computer science, software engneering Q1.

12. **Y. Ben Asher**, "*Optical Routing in Meshes Using the Duplication Model*", Journal of Parallel and Distributed Computing (JPDC) Vol. 41, pp. 36-41, 1997.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

13. **Y. Ben Asher** and I. Newman, "*Geometric Approach for Optimal Routing on Mesh with Buses*", Journal of Computer and System Sciences (JCSS) Vol. 54, No. 3, pp. 475-486, 1997.
IF=1.58 IF5y=1.59 14/51 computer science, theory&methods Q1.

14. **Y. Ben Asher** and A. Schuster, "*Single Step Undirected Reconfigurable Networks*", VLSI desgines, Special Issue High-Performance Bus-Based Architectures, Vol. 9, No. 1, pp. 17-28, 1999.
IF=0.13 IF5y=N.A 44/44 computer science, theory&methods Q4.

15. **Y. Ben Asher**, E. Farchi[#] and I. Newman, "*Optimal Search in Trees*", Society for Industrial and Applied Mathematics (SIAM) Journal on Computing Vol. 28, No. 6, pp. 2090-2102, 1999.
IF=0.84 IF5y=1.35 63/105 computer science, theory&methods Q2.
IF=1.00 IF5y=N.A 10/61 computer science, theory&methods Q1 (1999).

16. **Y. Ben Asher** and E. Stein[#], "*Basic Results in Automatic Transformations of Shared Memory Parallel Programs into Sequential Programs*", Journal of Supercomputing Vol. 17, No. 2 pp. 143-165, 2000.
IF=1.08 IF5y=1.01 23/51 computer science, theory&methods Q2.

17. **Y. Ben Asher** and G. Haber[#], "*Parallel Solutions of Simple Indexed Recurrence Equations*", IEEE Transactions on Parallel and Distributed Systems (TPDS) Vol. 12 No. 1. pp. 22-37, 2001.
IF=2.66 IF5y=2.74 9/105 computer science, theory&methods Q1.

18. **Y. Ben Asher** and D. Podvolny[#], "*Y-invalidate: a New Protocol for Implementing Weak Consistency in DSM Systems*", International Journal of Parallel Programming (IJPP) Vol. 29, No. 6, pp. 587-610, 2001.
IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

19. **Y. Ben Asher**, "*Distributed Routing of Ads and Bids through Random Walks in the IDOS System*", Journal of Parallel and Distributed Computing (JPDC), Vol. 61, No. 10, pp. 1456-1471, Oct 2001.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

20. **Y. Ben Asher**, "*The Parallel Client Server Paradigm*", Parallel Computing, Vol. 28, No. 2, pp. 503-523, Oct 2002.
IF=1.00 IF5y=1.66 53/105 computer science, theory&methods Q3.

21. **Y. Ben Asher** and E. Stein[#], "*Basic Algorithms for the Asynchronous Reconfigurable Mesh*", VLSI Design. Vol. 15, No. 1, pp. 441-454, 2002.
IF=0.13 IF5y=N.A 44/44 computer science, theory&methods Q4.

22. A. Agbaria, **Y. Ben Asher**, and I. Newman, "*CommunicationProcessor Tradeoffs in a Limited Resources PRAM*", Algorithmica. Vol. 34, pp. 276-297, 2002.
IF=0.79 IF5y=0.83 66/106 computer science, theory&methods Q3.

23. **Y. Ben Asher** and G. Haber[#], "*Efficient Parallel Solutions of Linear Algebraic Circuits*", Journal of Parallel and Distributed Computation (JPDC). Vol. 64, pp. 163-172, 2004.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

24. **Y. Ben Asher** and E. Farchi[#], "*Compact Representations of Search in Complex Domains*", International Game Theory Review Vol. 7, No.1 pp. 73–90, 2005.
IF=0.57 IF5y=0.71 92/123 statistics&probability Q3.

25. **Y. Ben Asher**, S. Berkovsky[#], E. Gelzin, E. Shmueli, A. Tammam, and M. Vilkhov, "*Using a J2EE Cluster for Parallel Computation of Join Queries in a Distributed Databases*", Journal of Digital Information Management, Vol 3, No. 2, pp. 76-81, 2005.
IF=N.A

26. **Y. Ben Asher**, and S. Berkovsky, "*Semantic Data Management in Peer-to-Peer E-Commerce Applications*", Journal on Data Semantics (JoDS), vol. 6, pp. 115-142, 2006.
IF=1.07 from ResearchGate

27. **Y. Ben Asher**, G. Haber and D. Citron, "*Overlapping Memory Operations with Circuit Evaluation in Reconfigurable Computing*", International Journal of Embedded Systems (IJES) , Vol. 2, No. 1 part 2, pp. 16-27, 2006.
    IF=N.A

28. **Y. Ben Asher** and D. Meisler[#], "*Towards a Source Level Compiler: Source Level Modulo Scheduling*", Springer LNCS 4444 special festschrift volume, pp. 328-360, 2007.
    IF=N.A

29. **Y. Ben Asher** and Ariel Tamam, "*Bartering Leftovers on the Internet*", Journal of Internet Technology (JIT) Vol. 8, No. 1, pp.33-40, 2007.
    IF=0.53 IF5y=0.38 125/144 computer science, information systems Q4.

30. **Y. Ben Asher**, S. Feldman[#], P. Gurfil and M. Feldman, "*IFAS: Interactive Flexible Ad Hoc Simulator*", Simulation Modelling Practice and Theory (SIMPAT), Vol. 15, No. 7, pp 817-830, 2007.
    IF=0.53 IF5y=N.A 54/83 computer science, software engineering Q3.

31. **Y. Ben Asher**, S. Feldman[#], P. Gurfil and M. Feldman, "*Distributed Decision and Control for Cooperative UAVs using Ad-Hoc Communication*", IEEE Transactions on Control Systems Technology, Vol. 16, No. 3, pp.511-516, 2008.
    IF=2.81 IF5y=3.41 30/257 engineering, electrical&electronics Q1.

32. **Y. Ben Asher** and M. Yuda[#], "*Source Level Merging of Independent Programs*", Journal of Parallel and Distributed Computation (JPDC), Vol. 69, No. 6, pp 521-531, 2009.
    IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

33. **Y. Ben Asher**, S. Feldman[#], P. Gurfil and M. Feldman, "*Scalability Issues in Ad-Hoc Networks: Metrical Routing Versus Table-Driven Routing*", Springer Journal of Wireless Personal Communications, Vol. 52, Issue 3, pp 423, 2010.
    IF=0.7 IF5y=0.66 63/82 telecommunication Q4.

34.[★] **Y. Ben Asher** and Jawad Haj-Yihia[#] "*Computing the correct Increment of Induction Pointers with application to loop unrolling*", ElseVier journal of systems architecture (JSA) Vol. 56, pp 654-666, 2010.
    IF=0.68 IF5y=0.74 34/51 computer science, hardware&architecture Q3.

35.[★] **Y. Ben Asher**, S. Feldman[#] and M. Feldman, "*Dynamic Multipath Allocation in Ad Hoc Networks*", The Computer Journal, Vol. 54, No. 2, pp 197-212, 2010.
    IF=1.0 IF5y=1.0 53/106 computer science, software engineering Q2.

36.[★] **Y. Ben Asher**, Nadav Rotem[#] and Eddie Schohat[#], "*Finding the Best Compromise in Compiling Compound Loops to Verilog*", ElseVier journal of systems architecture (JSA), Vol. 56, No. 9, pp. 474-486, 2010.
    IF=0.68 IF5y=0.74 34/51 computer science, hardware&architecture Q3.

37.[★] **Y. Ben Asher** and D. Meisler[#] and Nadav Rotem[#], "*Reducing Memory Constraints in Modulo Scheduling Synthesis for FPGAs*", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 3, No. 3, pp. , 2010.
    IF=0.5 IF5y=0.72 42/51 computer science, hardware&architecture Q4.

38.[★] Yosi Ben Asher and Mohsen Abu Saleh[#] "*Auctions by Price and Distance on Cellular Phones*", Journal of Electronic Commerce Research and Applications (ECRA), Vol. 10, No. 2, pp. 155-169, 2011.
    IF=2.13 IF5y=2.83 26/144 computer science, information systems Q1.

39.★ **Y. Ben Asher** and Nadav Rotem[#], "*Combining Static and Dynamic Array Detection for Binary Synthesis with Multiple Memory Ports*", Springer journal of Design Automation for Embedded Systems, Vol. 15, No. 1, pp. 1-18, 2011.
IF=0.09 IF5y=0.34 51/51 computer science, hardware&architecture Q4.

40.★ **Y. Ben Asher**, T. Gal[#], G. Haber and M. Zalmanovici, "*Refactoring Techniques for Aggressive Object Inlining in Java Applications*", Springer journal of Automated Software Engineering Vol. 19, No. 1, pp. 97-136, 2012.
IF=1.31 IF5y=1.59 32/106 computer science, software engineering Q2.

41.★ F. Abboud, **Y. Ben Asher**, Y. Sajrawi and E. Stein[#], "*Combining Height Reduction and Scheduling for VLIW Machines Enhanced with Three-Argument Arithmetic Operations*", Springer International Journal of Parallel Programming (IJPP) Vol 40, No. 5, pp 488-513, 2012. IF=0.5 IF5y=0.47 IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

42.★ **Y. Ben Asher** and Nadav Rotem[#], "*Block Unification IF-conversion for High Performance Architectures*", IEEE Computer Architecture Letters (CAL), Vol. 99, pp. 1, 2012.
IF=0.45 IF5y=0.94 45/51 computer science, hardware&architecture Q4.
IF=0.85 IF5y=NA 29/50 computer science, hardware&architecture Q3 (2012).

43.★ **Y. Ben Asher** and Nadav Rotem[#], "*Using Memory Profile Analysis for Automatic Synthesis of Pointers and General Memory References*", ACM Transactions on Embedded Computing Systems TECS, Vol 12, No. 3, pp. 68, 2013.
IF=0.71 IF5y=0.74 31/53 computer science, hardware&architecture Q3.

44.★ **Y. Ben Asher** and Nadav Rotem[#], "*Hybrid type legalization for a sparse SIMD instruction set*", ACM Transactions on architecture and code optimization (TACO), Vol 10, No. 3, pp.11, 2013.
IF=0.58 IF5y=0.64 37/53 computer science, hardware&architecture Q3.

45.★ **Y. Ben Asher** and Nadav Rotem[#], "*Benefits of Using Variable-Length Pipelined Operations in Highlevel Synthesis*", ACM Transactions on Embedded Computing Systems (TECS), Vol. 13, No. 3, pp. 52, 2013.
IF=0.71 IF5y=0.74 31/53 computer science, hardware&architecture Q3.

46.★ **Y. Ben Asher**, R. Meldiner[#] and N. Rotem[#], "*Optimizing Wait-States in the Synthesis of Memory References with Unpredictable Latencies*", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 6, No. 4, pp. 19, 2013.
IF=0.5 IF5y=0.72 42/51 computer science, hardware&architecture Q4.

47.★ J. Haj-Yihia[#], **Yosi Ben-Asher**, E. Rotem, A. Yassin and R. Ginosar, "*Compiler-Directed Power Management for Superscalars*", ACM Transactions on architecture and code optimization (TACO), Vol 11, No. 4, pp. 48:1-48:21, 2014.
IF=0.58 IF5y=0.64 37/53 computer science, hardware&architecture Q3.

48.★ **Y. Ben Asher** and Cfir Aguston[#] and Gadi Haber, "*Parallelization Hints via Code Skeletonization*", IEEE Transactions on Parallel and Distributed Systems (TPDS), Vol 26, No. 11, pp. 9:3099-3107, 2015.
IF=2.66 IF5y=2.74 9/105 computer science, theory&methods Q1.

49.★ **Y. Ben-Asher**, and E. Stein, "*Adaptive Booth Algorithm for Three-integers Multiplication for Reconfigurable Mesh*", World Sience Journal of interconnection networks (JOIN), Vol 16, No. 1, pp. 25pages, 2016.
IF=N.A

50.★ J. Haj-Yihia[#], **Y. Ben-Asher**, A. Mendelson, A. Yassin, *"Fine-grain Power Breakdown of Modern Out-Of-Order Cores and its implications on Skylake based systems"*, ACM Transactions on architecture and code optimization (TACO), 2016.
IF=0.58 IF5y=0.64 37/53 computer science, hardware&architecture Q3.