CURRICULUM VITAE

Yosi Ben-Asher

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1 Personal Details

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2 Higher Education

a Undergraduate and Graduate Studies

Period of Study	Name of Institution and Department	Degree	Date of Degree
1985 1990	Hebrew University, computer science	Ph.D	4.6.1990
1983-1984	Hebrew University, computer science	M.Sc	1.6.1984
1979-1982	Hebrew University, Physics	B.Sc	1.5.1982

b Post-Doctoral Studies

Period of Study	Name of Institution, Department	Host	Year of completion
1991	Hebrew University, computer science	L. Rudolph	1991

3 Academic Ranks

Dates	Name of Institution and Department	Rank/Position
1985-1987	Courant Institute, NYU Ultracomputer lab	Visiting Position (during summers)
1992-1996	Dep. of Computer Science University of Haifa	Lecturer
1996-2008	Dep. of Computer Science University of Haifa	Senior Lecturer (Tenure)
2009-	Dep. of Computer Science University of Haifa	Associate Professor

Note: ★ represents activities and publications since promotion to Associate Prodessor.

4 Offices in university academic administration

2011-2016 Faculty teaching committee.

5 Scholarly Positions and Activities Outside the University

5A. ★ SOP Transactions on Wireless Communications: editorial board (2014).

5B. Invitations to review journal manuscripts: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems ★ ,
Journal of Parallel and Distributed Computing ★ ,
Electronic Commerce Research and Applications ★ ,
The journal of supercomputing ★ ,
IEEE Transactions on Parallel and Distributed Systems (TPDS) ★ ,
Journal of Circuits, Systems and Computers ★ ,
IEEE Transactions on Parallel and Distributed Systems ★ ,
Transactions on wireless communications ★ ,
Oxford the Computer Journal ★ ,
European Journal of Operational Research ★ ,
IEEE Transactions on Computers,
Theoretical computer science (TCS),
Journal of Electronic Commerce Research and Applications,
International Journal of Emerging Sciences (IJES),

and Journal of Software Testing, Verification and Reliability.

5C. Other reviews: Msc+Phd thesis evaluation for the: ★ Technion CS and EE, Hebrew University CS, and ⋆ Ben Gurion University.

5D. Commercial consulting:

1999 Consultant at IBM Haifa Research Labs

2003-2004 Consultant at Starcore (compiler group) Azur.

★ [2011] Taught a course on compiler optimizations at Intel IDC in Haifa.

5E. Program committees:

- The 19th ACM International Conference on Supercomputing 2005.
- Workshop in Parallel and Distributed Systems Testing and Debugging 2004,2005.
- 4'th IEEE international conference on information technology research and education 2006.
- ★ Workshop on Parallel and Distributed Systems: Testing, Analysis, and Debugging 2007-2009
- ★ ESA'09: The 2009 International Conference on Embedded Systems.
- ★ External Review Committee, Design Automation Conference (DAC) 2013-15.
- ★ Intel IDC, Compiler, Architecture and Tools Conference 2014.
- ★ Intel IDC, Compiler, Architecture and Tools Conference 2015.

6 Participation in Scholarly Conferences

a Active Participation.

I participated and presented works in most of the conferences of section f.

b Organization of Conferences or Session.

None.

7 Invited Lectures

Dagstul seminars are closed meetings in which a committee invites a small number of experts to participate and give talks. Being invited to these meetings is very prestigious and the inviting institutions cover the costs of the participants during the meetings.

Research grants

Date	Place of Lecture	Name of Forum	Presentation/Comments
1997	Dagstuhl	Dagstuhl seminar on Parallel and Distributed Algorithms	CommunicationProcessor Tradeoffs
2000	Dagstuhl	Dagstuhl seminar on Dynamically Reconfigurable Architectures	Complexity of the Reconfigurable Mesh
2003	IBM Haifa Research Labs	Seminar	Overlapping Memory Operations with Circuit Evaluation in Hardware Compilation
2005	IBM Haifa Research Labs	Seminar	Source Level Modulo Scheduling
2006	Dagstuhl	Festschrift and celebration in honor of Reinhard Wilhelm	Source level Modulo scheduling
2006	Hi-Tech Convention Center TLV	DSP Conference	Highlevel Synthesis

8 Colloquium Talks

I have given several colloquium talks about the works described in the list of publications. These include: the Technion, Hebrew university, University of Haifa, Weizmann Institute and Ben-Gorion University, NYU, IBM, Lucent, IBM Haifa Research Lab, Georgia Inst. of Technology, UIUC and Saarbrucken university.

9 Research Grants

All the Co-Researchers are PI.

Role in Research	Other Researchers AU PI	Topic	Funded by C=copetative fund	Amount	Year
PI	Assaf Schuster (Technion), Roy Fridman (Technion), Israel ben Shaul (Technion), Danny Dolev (Hebrew University) and Dror Feitelson (Hebrew University)	HPARC system	Ministry of Science (C)	260,000 NIS	1998-2000
PI	Moni Naor (Weizaman Institute), Dov Monderer (Technion), Doron Sonsino (Technion) and Moshe Tennenholtz (technion)	protocol for Electronic Commerce over the Internet	Ministry of Science (C)	260,000 NIS	1998-2000
PI		VLIW scheduling techniques	A Magnet grant from SWR consortium (C)	585,000 NIS	2001-2003
PI		Peer-to-Peer systems	Caesarea Rothschild Foundation (C.R.I)	20,000 USD	2002-2003
PI		Ad-Hoc routing algorithms to the avionic industry	A magneton with the Avionic Industry (C)	total 1,200,000 NIS	2004-2005
★ PI	Ran Ginosar (Technion EE)	High Level Synthesis to Large Nets of Carbon Nanotube FETs	Ministry Of Science (C)	600,000 NIS	2009-2011
★ PI		compiling programs to a netlist of optical switches	Israel Science Foundation (ISF) (C)	345,000 NIS	2009-2011
★ PI		1K Manycore FPGA Shared Memory Architecture for SOC Demonstrating Deep Packet Inspection	Ministry Of Science (C)	500,000 NIS	2013-2016

10 Scholarships, Awards and Prizes

1988,1989 Leibniz Scholarship, facilitating doctoral studies and parallel processing research.

1990 Eschol Post-Doctorate Scholarship of the ministry of science and development, for optical computing.

1991 Davis Post-Doctorate Scholarship of the CS. Department in the Hebrew University.

11 Teaching

a Courses taught in recent years

Year	Name of Course	Type of Course	Degree	Number of Students
1998	Introduction to Digital Design	Lecture	B.Sc.	∼50
2001	Introduction to computer science	Lecture	B.Sc.	∼ 60
2004	Distributed File Systems	Lecture	M.Sc	∼30
2001,2002	Advanced client/server systems	Lecture+Lab	M.Sc+B.Sc	∼30
2002	Automatic parallelization and software pipelining	Seminar, M.Sc	∼30	
2002	Distributed shared memory systems	Seminar	M.Sc	∼30
2003	Parallel Algorithms	Lecture	M.Sc+B.Sc.	∼30
2005	Advance laboratory in operating systems	Lecture+Lab	B.Sc+M.Sc	∼30
2006	Lab in Parallel Processing	Lecture	M.Sc+B.Sc	∼30
2006-2008	Lab in compiler optimizations	Lecture+Lab	B.Sc+M.Sc	∼30
2009	Distributed web programming	Lecture	M.Sc+B.Sc	∼30
★ 2004-2014	Advanced compiler optimizations (every two years)	Lecture	B.Sc+M.Sc	∼30
★ 2007-2016	Lab in chip design	Lecture+Lab	B.Sc+M.Sc	∼30
★ 2003-2016	Practical Parallel Programming (every two years)	Lecture	M.Sc+B.Sc	∼35
★ 1994-2016	Compiler design	Lecture	B.Sc.	80-120

b Supervision of graduate students

Name of Student	Title of Thesis	Degree	Date of completion/ in Progress	Students' Achievements
Eitan Farchi	Testing games	Ph.D	1998	see conferences(f) 19, 44, and journals(d) 5, 20, 29
Gady Haber	Parallel Evaluation of Sequential Code	Ph.D	2003	see conferences(f) 29, 31, 35, 39, and journals(d) 26, 19, 23
Sharoni Feldman	Study of Metrical Routing in Ad Hoc Networks	Ph.D	2007	see conferences(f) 34, 35, 36, 45, and journals(d) 35, 36, 38, 40
★ Esti Stein	Numeric computations on the reconfigurable mesh	Ph.D	2010	see conferences(f) 26, 47, and journals(d) 26
★ Nadav Rotem	Synthesis of circuits directed by memory profile information	Ph.D	2013	see conferences(f) 48, 49, 49, and journals(d) 44,47, 48, 49
★ Jawad Haj-Yihia	Power reducuctions via compiler optimizations	Ph.D	2017	see conferences(f) 62, 63 and journals(d) 39, 52
★ Vladislav Tartakovskiy	Syntehsis of circuits that use ballistic deflection transistors and optical switches	Ph.D	in progress	see conferences(f) 53, 59
★ Ahmad Yasin	Analysis of Big-Data applications in Large Scale Cloude Systems	Ph.D	in progress	see conferences(f) 63, 61
★ Irina Lipov	Optimizing Spark Programs	Ph.D	in progress	

Name of Student	Title of Thesis	Degree	Date	Students' Achievements
Adnan Agbaria (joint supervision with I. Newman)	Parallel algorithms with limmited shared memory	M.Sc	1997	see conferences 24, journals 27
Esti Stein	Sequential transformation of parallel programs	M.Sc	1997	see conferences 33, journals 21
Vitaly Grachenko	Parallel systems in a network of workstations	M.Sc	1999	-
Gabriel Mizrahi	The hashing approach to the Internet File System problem	M.Sc	2002	-
Dimitry Giver	HparC: Programming Parallel Applications Over the Internet	M.Sc	2002	conferences 51
Dimitry Podvolny	Y-invalidate: a New Protocol for Implementing Weak Consistency in DSM Systems	M.Sc	2003	see journals 23
Shlomo Berkovsky	peer2peer systems	M.Sc	2005	see conferences 29, 30, 31, journals 30, 31
Yaniv Eitany	software testing (joint with E. Farchi)	M.Sc	2006	see conferences 27
Danny Meisler	Source level modulo scheduling	M.Sc	2006	see conference 37, journals 42
Moshe Yuda	Source Level Merging of independent programs	M.Sc	2007	see conferences 41, journals 37
★ Eddie Shochat	Finding the Best Compromise in Compiling Compound Loops to Verilog	M.Sc	2008	see conferences 43, journals 41
★ Jawad Haj-Yihia	Source level Unrolling of Loops Containing Pointers and Array References	M.Sc	2008	journals 39
★ Nadav Rotem	Synthesis of pipelined multiplications	M.Sc	2008	see conferences 46 journals 50
★ Mohsen Abu Saleh	Auctions by Price and Distance on Cellular Phones	M.Sc	2009	journals 43
★ Tomer Gal (joint with G. Haber)	Refactoring Techniques for Aggressive Object Inlining in Java Applications	M.Sc	2009	journals 45
★ Ron Meldiner	High level synthesis with unknown delays of memory references	M.Sc	2011	see conferences 52
★ Gil Kulish	Combining Cache Aware Scheduling with Lazy Threads	M.Sc	2011	conferences 54
★ Yehuda Ezra	Proactive Channel Allocation for Ad-Hoc Networks	M.Sc	2012	conferences 55
★ Vladislav Tartakovskiy	Optical Spice simulations of Branching programs	M.Sc	2012	conferences 53
★ Ahmad Yasin (joint supervi-	Map-Reduce Characterization	M.Sc	2014	61

Name of Student	Title of Thesis	Degree	Date	Students' Achievements
★ Cfir Aguston	Parallelization Hints via Code Skeletonization	M.Sc	2013	conferences 56 journals 53
★ Gil Rapaport	Design of effcient vectorized code	M.Sc	2013	conferences 65
★ Irena Lipov	Time Area scheduling (TAS): Unifying Scheduling with Place and Route for Highlevel Synthesis	M.Sc	2013	-
★ Dror Tiv	Using Multi-op Instructions As a Way to Generate ASIPs with Optimized Pipeline Structure	M.Sc	2014	conferences 59
★ Yousef Sajrawi	1K Manycore FPGA Shared Memory Architecture for SoC	M.Sc	2013	conferences 58, 64
★ Nir Rozen	Parallelized Snort Defense against Distributed Denial of Service Flooding	M.Sc	in progress	-

PUBLICATIONS

a Ph.D Dissertation

The thesis (Hebrew, 4.6.1990, 100 pages): " M&P a non Procedural Parallel Programming Language, Based on Set Theory". The thesis was supervised by prof. M. Snir from Chicago, Illinois (former IBM T.J. Watson Research Center).

The thesis introduces the idea of a parallel language (M&P) capable of using the joint power of millions of processors. Programming in this language is based on Cartesian products of groups, where each element of a group is a data structure accessible via properties.

b Scientific Books (Refereed)

★ **Y. Ben Asher**, *Multicore Programming Using the Parc Language*, Book, 361 pages, published by Springer, 2012.

c Monographs

none

d Articles in Refereed Journals

Names of authors are in alphabetical order. IF were taken from ISI Journal citation Reports (JCR) and are all from 2015 or the latest year available. Some journals are not covered by ISI JCR and I used ResearchGate instead. # indicates that the author is my student.

1. S. Nirenburg and **Y. Ben Asher**, "*HUHU: The Hebrew University Hebrew Understander*", Comput. Languages Vol 9, pp. 161-182 1984.
   IF=1.25 IF5y=N.A 19/78 computer science, software engineering Q1.

2. **Y. Ben Asher**, D. Peleg, R. Ramaswami and A. Schuster, "*The Power of Reconfiguration*", Journal of Parallel and Distributed Computing (JPDC), Vol. 13, pp. 139-153, 1991.
   IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

3. **Y. Ben Asher** and A. Schuster, "*Ranking on Reconfigurable Networks*", Parallel Processing Letters, vol. 1, no. 2, pp. 149-156, 1991.
   IF=1.12 (from ResearchGate 2012)

4. **Y. Ben Asher**, D. Egosi and A. Schuster, "*2-D SIMD Algorithms for Perfect Shuffle Networks*", Journal of Parallel and Distributed Computation (JPDC), Volume 16, pp.

250-257, 1992.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

5. **Y. Ben Asher** and E. Farchi, "*Using True Concurrency to Model Execution of Parallel Programs*", International Journal of Parallel Programming (IJPP), Vol. 22 No. 4, pp. 375-407, 1994.
IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

6. **Y. Ben Asher** and A. Schuster, "*The Complexity of Data-Reduction on the Reconfigurable Linear Array*", Journal of Algorithms Vol. 18 pp. 322-375, 1995.
IF=1.38 IF5y=1.35 54/117 computer science, theory&methods Q2.

7. **Y. Ben Asher**, "*The Cartesian Product Problem and Implementing Production Systems on Reconfigurable Meshes*", Parallel Processing Letters, Vol. 5 No. 1, pp. 49-61, 1995.
IF=1.12 (from ResearchGate 2012)

8. **Y. Ben Asher**, D. Gordon and A. Schuster, "*Efficient Self Simulation Algorithms in Reconfigurable Arrays*", Journal of Parallel and Distributed Computing (JPDC), Vol. 30, pp. 1-22, 1995.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

9. **Y. Ben Asher**, A. Schuster and J.F. Sibeyn, "*Load Balancing: A Programmer's Approach or The Impact of Task-Length Parameters on the Load Balancing Performance of Parallel Programs.*", International Journal of High-Speed Computing, Vol. 7, No. 2, pp. 303-325, 1995.
IF=0.15 IF5y=N.A 65/71 computer science, theory&methods Q4.

10. **Y. Ben Asher**, K. Lange, D. Peleg and A. Schuster, "*The Complexity of Reconfiguring Network Models*", Information and Computation, Vol. 21, (1) pp. 41-58, 1995.
IF=0.87 IF5y=0.91 60/105 computer science, theory&methods Q2.

11. **Y. Ben Asher**, G. Rünger, A. Schuster and R. Wilhelm, "*2DT-FP: An FP Based Programming Language for Efficient Parallel Programming of Multiprocessor Networks*", International Journal of Parallel Programming (IJPP), Vol 23, No 5, pp. 389-422, 1995.
IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

12. **Y. Ben Asher** and I. Newman, "*Decision Trees with Boolean Threshold Queries*", Journal of Computer and System Sciences (ICSS), Vol. 51, No. 3, pp. 495-502, 1995.
IF=1.58 IF5y=1.59 14/51 computer science, hardware&architectures Q2.

13. **Y. Ben Asher**, and A. Schuster, "*Low Crosstalk Address Encodings for Optical Message Switching Systems*", Parallel Processing Letters, vol. 6, no. 1, pp. 87-100, Feb. 1996.
IF=1.12 (from ResearchGate 2012)

14. **Y. Ben Asher**, D. Feitelson and L. Rudolph, "*Parc, An extension of* C ", Journal of Software practice & Experience, Vol. 26, No. 5, pp. 581-612, 1996.
IF=1.0 IF5y=1.25 76/106 computer science, software engineering Q3.

15. **Y. Ben Asher**, A. Cohen and A. Schuster, "*Tradeoffs Between Size and Time in Reconfigurable Meshes*", Parallel processing letters (PPL), volume 6 number 2, 1996.
IF=1.12 (from ResearchGate 2012)

16. G. Haber and **Y. Ben Asher**, "*On the Usage of simulators to detect inefficiency of parallel programs caused by "bad" schedulings: the SIMPARC approach*", Journal of Systems and Software, Vol. 33, No. 3, pp. 313-333, 1996.
IF=1.42 IF5y=1.76 24/106 computer science, software engneering Q1.

17. **Y. Ben Asher**, "*Optical Routing in Meshes Using the Duplication Model*", Journal of Parallel and Distributed Computing (JPDC) Vol. 41, pp. 36-41, 1997.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

18. **Y. Ben Asher** and I. Newman, "*Geometric Approach for Optimal Routing on Mesh with Buses*", Journal of Computer and System Sciences (JCSS) Vol. 54, No. 3, pp. 475-486, 1997.
IF=1.58 IF5y=1.59 14/51 computer science, theory&methods Q1.

19. **Y. Ben Asher** and A. Schuster, "*Single Step Undirected Reconfigurable Networks*", VLSI desgines, Special Issue High-Performance Bus-Based Architectures, Vol. 9, No. 1, pp. 17-28, 1999.
IF=0.13 IF5y=N.A 44/44 computer science, theory&methods Q4.

20. **Y. Ben Asher**, E. Farchi[#] and I. Newman, "*Optimal Search in Trees*", Society for Industrial and Applied Mathematics (SIAM) Journal on Computing Vol. 28, No. 6, pp. 2090-2102, 1999.
IF=0.84 IF5y=1.35 63/105 computer science, theory&methods Q2.
IF=1.00 IF5y=N.A 10/61 computer science, theory&methods Q1 (1999).

21. **Y. Ben Asher** and E. Stein[#], "*Basic Results in Automatic Transformations of Shared Memory Parallel Programs into Sequential Programs*", Journal of Supercomputing Vol. 17, No. 2 pp. 143-165, 2000.
IF=1.08 IF5y=1.01 23/51 computer science, theory&methods Q2.

22. **Y. Ben Asher** and G. Haber[#], "*Parallel Solutions of Simple Indexed Recurrence Equations*", IEEE Transactions on Parallel and Distributed Systems (TPDS) Vol. 12 No. 1. pp. 22-37, 2001.
IF=2.66 IF5y=2.74 9/105 computer science, theory&methods Q1.

23. **Y. Ben Asher** and D. Podvolny[#], "*Y-invalidate: a New Protocol for Implementing Weak Consistency in DSM Systems*", International Journal of Parallel Programming

(IJPP) Vol. 29, No. 6, pp. 587-610, 2001.
IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

24. **Y. Ben Asher**, "*Distributed Routing of Ads and Bids through Random Walks in the IDOS System*", Journal of Parallel and Distributed Computing (JPDC), Vol. 61, No. 10, pp. 1456-1471, Oct 2001.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

25. **Y. Ben Asher**, "*The Parallel Client Server Paradigm*", Parallel Computing, Vol. 28, No. 2, pp. 503-523, Oct 2002.
IF=1.00 IF5y=1.66 53/105 computer science, theory&methods Q3.

26. **Y. Ben Asher** and E. Stein#, "*Basic Algorithms for the Asynchronous Reconfigurable Mesh*", VLSI Design. Vol. 15, No. 1, pp. 441-454, 2002.
IF=0.13 IF5y=N.A 44/44 computer science, theory&methods Q4.

27. A. Agbaria, **Y. Ben Asher**, and I. Newman, "*CommunicationProcessor Tradeoffs in a Limited Resources PRAM*", Algorithmica. Vol. 34, pp. 276-297, 2002.
IF=0.79 IF5y=0.83 66/106 computer science, theory&methods Q3.

28. **Y. Ben Asher** and G. Haber#, "*Efficient Parallel Solutions of Linear Algebraic Circuits*", Journal of Parallel and Distributed Computation (JPDC). Vol. 64, pp. 163-172, 2004.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

29. **Y. Ben Asher** and E. Farchi#, "*Compact Representations of Search in Complex Domains*", International Game Theory Review Vol. 7, No.1 pp. 73–90, 2005.
IF=0.57 IF5y=0.71 92/123 statistics&probability Q3.

30. **Y. Ben Asher**, S. Berkovsky#, E. Gelzin, E. Shmueli, A. Tammam, and M. Vilkhov, "*Using a J2EE Cluster for Parallel Computation of Join Queries in a Distributed Databases*", Journal of Digital Information Management, Vol 3, No. 2, pp. 76-81, 2005.
IF=N.A

31. **Y. Ben Asher**, and S. Berkovsky, "*Semantic Data Management in Peer-to-Peer E-Commerce Applications*", Journal on Data Semantics (JoDS), vol. 6, pp. 115-142, 2006.
IF=1.07 from ResearchGate

32. **Y. Ben Asher**, G. Haber and D. Citron, "*Overlapping Memory Operations with Circuit Evaluation in Reconfigurable Computing*", International Journal of Embedded Systems (IJES) , Vol. 2, No. 1 part 2, pp. 16-27, 2006.
IF=N.A

33. **Y. Ben Asher** and D. Meisler#, "*Towards a Source Level Compiler: Source Level Modulo Scheduling*", Springer LNCS 4444 special festschrift volume, pp. 328-360, 2007.
IF=N.A

34. **Y. Ben Asher** and Ariel Tamam, "*Bartering Leftovers on the Internet*", Journal of Internet Technology (JIT) Vol. 8, No. 1, pp.33-40, 2007.
IF=0.53 IF5y=0.38 125/144 computer science, information systems Q4.

35. **Y. Ben Asher**, S. Feldman#, P. Gurfil and M. Feldman, "*IFAS: Interactive Flexible Ad Hoc Simulator*", Simulation Modelling Practice and Theory (SIMPAT), Vol. 15, No. 7, pp 817-830, 2007.
IF=0.53 IF5y=N.A 54/83 computer science, software engineering Q3.

36. **Y. Ben Asher**, S. Feldman#, P. Gurfil and M. Feldman, "*Distributed Decision and Control for Cooperative UAVs using Ad-Hoc Communication*", IEEE Transactions on Control Systems Technology, Vol. 16, No. 3, pp.511-516, 2008.
IF=2.81 IF5y=3.41 30/257 engineering, electrical&electronics Q1.

37. **Y. Ben Asher** and M. Yuda#, "*Source Level Merging of Independent Programs*", Journal of Parallel and Distributed Computation (JPDC), Vol. 69, No. 6, pp 521-531, 2009.
IF=1.17 IF5y=1.2 36/102 computer science, theory&methods Q2.

38. **Y. Ben Asher**, S. Feldman#, P. Gurfil and M. Feldman, "*Scalability Issues in Ad-Hoc Networks: Metrical Routing Versus Table-Driven Routing*", Springer Journal of Wireless Personal Communications, Vol. 52, Issue 3, pp 423, 2010.
IF=0.7 IF5y=0.66 63/82 telecommunication Q4.

39.★ **Y. Ben Asher** and Jawad Haj-Yihia# "*Computing the correct Increment of Induction Pointers with application to loop unrolling*", ElseVier journal of systems architecture (JSA) Vol. 56, pp 654-666, 2010.
IF=0.68 IF5y=0.74 34/51 computer science, hardware&architecture Q3.

40.★ **Y. Ben Asher**, S. Feldman# and M. Feldman, "*Dynamic Multipath Allocation in Ad Hoc Networks*", The Computer Journal, Vol. 54, No. 2, pp 197-212, 2010.
IF=1.0 IF5y=1.0 53/106 computer science, software engineering Q2.

41.★ **Y. Ben Asher**, Nadav Rotem# and Eddie Schohat#, "*Finding the Best Compromise in Compiling Compound Loops to Verilog*", ElseVier journal of systems architecture (JSA), Vol. 56, No. 9, pp. 474-486, 2010.
IF=0.68 IF5y=0.74 34/51 computer science, hardware&architecture Q3.

42.★ **Y. Ben Asher** and D. Meisler# and Nadav Rotem#, "*Reducing Memory Constraints in Modulo Scheduling Synthesis for FPGAs*", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 3, No. 3, pp. , 2010.
IF=0.5 IF5y=0.72 42/51 computer science, hardware&architecture Q4.

43.★ Yosi Ben Asher and Mohsen Abu Saleh# "*Auctions by Price and Distance on Cellular Phones*", Journal of Electronic Commerce Research and Applications (ECRA), Vol. 10, No. 2, pp. 155-169, 2011.
IF=2.13 IF5y=2.83 26/144 computer science, information systems Q1.

44.★ **Y. Ben Asher** and Nadav Rotem#, "*Combining Static and Dynamic Array Detection for Binary Synthesis with Multiple Memory Ports*", Springer journal of Design Automation for Embedded Systems, Vol. 15, No. 1, pp. 1-18, 2011.
IF=0.09 IF5y=0.34 51/51 computer science, hardware&architecture Q4.

45.★ **Y. Ben Asher**, T. Gal#, G. Haber and M. Zalmanovici, "*Refactoring Techniques for Aggressive Object Inlining in Java Applications*", Springer journal of Automated Software Engineering Vol. 19, No. 1, pp. 97-136, 2012.
IF=1.31 IF5y=1.59 32/106 computer science, software engineering Q2.

46.★ F. Abboud, **Y. Ben Asher**, Y. Sajrawi and E. Stein#, "*Combining Height Reduction and Scheduling for VLIW Machines Enhanced with Three-Argument Arithmetic Operations*", Springer International Journal of Parallel Programming (IJPP) Vol 40, No. 5, pp 488-513, 2012. IF=0.5 IF5y=0.47 IF=0.68 IF5y=0.64 75/105 computer science, theory&methods Q3.

47.★ **Y. Ben Asher** and Nadav Rotem#, "*Block Unification IF-conversion for High Performance Architectures*", IEEE Computer Architecture Letters (CAL), Vol. 99, pp. 1, 2012.
IF=0.45 IF5y=0.94 45/51 computer science, hardware&architecture Q4.
IF=0.85 IF5y=NA 29/50 computer science, hardware&architecture Q3 (2012).

48.★ **Y. Ben Asher** and Nadav Rotem#, "*Using Memory Profile Analysis for Automatic Synthesis of Pointers and General Memory References*", ACM Transactions on Embedded Computing Systems TECS, Vol 12, No. 3, pp. 68, 2013.
IF=0.71 IF5y=0.74 31/53 computer science, hardware&architecture Q3.

49.★ **Y. Ben Asher** and Nadav Rotem#, "*Hybrid type legalization for a sparse SIMD instruction set*", ACM Transactions on architecture and code optimization (TACO), Vol 10, No. 3, pp.11, 2013.
IF=0.58 IF5y=0.64 37/53 computer science, hardware&architecture Q3.

50.★ **Y. Ben Asher** and Nadav Rotem#, "*Benefits of Using Variable-Length Pipelined Operations in Highlevel Synthesis*", ACM Transactions on Embedded Computing Systems (TECS), Vol. 13, No. 3, pp. 52, 2013.
IF=0.71 IF5y=0.74 31/53 computer science, hardware&architecture Q3.

51.★ **Y. Ben Asher**, R. Meldiner# and N. Rotem#, "*Optimizing Wait-States in the Synthesis of Memory References with Unpredictable Latencies*", ACM Transactions on

Reconfigurable Technology and Systems (TRETS), Vol. 6, No. 4, pp. 19, 2013.
IF=0.5 IF5y=0.72 42/51 computer science, hardware&architecture Q4.

52.★ Jawad Haj-Yihia#, **Yosi Ben-Asher**, E. Rotem, A. Yassin and R. Ginosar, "*Compiler-Directed Power Management for Superscalars*", ACM Transactions on architecture and code optimization (TACO), Vol 11, No. 4, pp. 48:1-48:21, 2014.
IF=0.58 IF5y=0.64 37/53 computer science, hardware&architecture Q3.

53.★ **Y. Ben Asher** and Cfir Aguston# and Gadi Haber, "*Parallelization Hints via Code Skeletonization*", IEEE Transactions on Parallel and Distributed Systems (TPDS), Vol 26, No. 11, pp. 9:3099-3107, 2015.
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Appeared as a chapter for the book "Heterogeneous Computing"
Mary M. Eshaghian (Ed.), Artech House, 1996, pp. 303-334, ISBN 0-89006-552-7.
This chapter has been thoroughly refereed, and includes new results on the subject of Heterogeneous Computing.

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66.★ **Y. Ben Asher** and Irina Lipov and Vladislav Tartakovsky and Dror Tiv, *Generating ASIPs with Reduced Number of Connections to the Register-file*, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XI), 2015.

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g Entries in Encyclopedias

h Other Scientific Publications

i Other Works and Publications

i.1 Patents:

1. System and method for classifying, publishing, searching and locating electronic documents
   Patent number: 8799289
   Type: Grant
   Filed: September 1, 2005
   Issued: August 5, 2014
   Assignee: Carmel-Haifa University Economic Corp. Ltd.
   Inventors: Yosef Ben Asher, Shlomo Berkovsky

2. UAV decision and control system
   Patent number: 8186589
   Type: Grant
   Filed: January 10, 2007
   Issued: May 29, 2012
   Assignees: Carmel-Haifa University Economic Corporation Ltd., Technion Research and Development Foundation Ltd.
   Inventors: Yosef Ben Asher, Sharoni Feldman, Pinchas Gurfil

3. Method of Routing Speech Packets in an Ad Hoc Network
   Patent number: 7738402
   Type: Grant
   Filed: December 21, 2005
   Issued: June 15, 2010
   Assignee: Carmel-Haifa University Economic Corp. Ltd.
   Inventors: Sharoni Feldman, Yosi Ben Asher

j Submitted for Publication

1. ★ Y. Ben-Asher and E. Stein, *Adaptive Booth Algorithm for Three-integers Multiplication for Reconfigurable Mesh* submitted to ACM Transactions on Reconfigurable Technology TRETS, 8 pages, (IF=0.4 IF5y=NA).

2. ★ Y. Ben-Asher and Y. Ezra, *PCA - Proactive Channel Allocation for Multi-Hop Ad-Hoc Networks* submitted to Journal of Computer and System Sciences JCSS, 32 pages, (IF=1.0 IF5y=1.26).

3. ★ Yosi Ben Asher, Eldar Fisher, Gady Haber and Vladislav Tartakovsky *Fast Evaluation of Boolean Circuits Based on Two-Players Game and Optical Connectivity Circuit* submitted to Journal of Computer and System Sciences JCSS, 30 pages, (IF=1.0 IF5y=1.26).

4. ★ Y. Ben-Asher and Gil Kulish, *Combining Cache Aware Scheduling with Lazy Threads* Submitted to IEEE Transactions on Parallel and Distributed Systems TPDS, 25 pages, (IF=2.1 IF5y=2.6).

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k Summary of my Activities and Future Plans

My research is mainly in compiler-optimizations, highlevel synthesis, parallelism and reconfigurable networks. This is a highly practical field of research wherein the main effort is to develop new compilation techniques targeting hardware circuits. Current research directions and systems are as follows:

C-to-Verilog compilation - We address issues such as scheduling, unexpected memory latencies, profiled-based memory configuration and the use of loop transformations. Two systems have been developed:

- Htiny a synthesizing system that is based on loop-transformations and uses modulo-scheduling to maximize parallelism.
- SystemRacer an LLVM extension that uses memory-profile to determine an optimized memory configuration for the resulting Verilog modules.
- IY system an LLVM based compiler from C to Verilog minimizing both time and wire-lengths.

Parallel Programming- We are developing a parallel programming system that is based on ParC (similar to OpenMP but more flexible) combining cache-aware scheduling, compiler directed lazy-threading and vectorization.

1K manycore-cpu : Is a shared memory architecture that we are developing for embedded systems that use network-on-chip to route packets from cores to memory modules and back. By this we follow original theoretical construction of PRAM machines via universal hashing proposed a decade ago. Goal is to create a uniform pure-software infrastructure for SOC applications. Currently we were able to synthesize 1024-cores over the Virtex-7 FPGA with clock-rate that is similar to an ARM-cpu.

The Ocpu - An ASIP obtaining high IPC values for specific programs. Goal to use Ocpu units in SOC applications. We study the use of graph-partitioning techniques to automatically synthesize thick pipeline architectures wherein each pipeline unit contains several memory and arithmetic stages. Preliminary results show that high throughput and low power consumption can be achieved using these large multi-op instructions.

P2NC- We developed a heuristic algorithmic technique to practically speed up the evaluation of boolean circuits to log-depth parallel steps. In each step two players (AND-player/OR-player) reconfigure their AND/OR-gates preventing 1/0 input signals from reaching their gate. Failing to do so for a given gate implies that the value of this gate is determined. The algorithm has been evaluated using a compiler from C-code to boolean circuits.

BC2BP - An effort to develop a heuristic algorithm and a system to convert boolean circuits (BCs) to branching programs (BPs) maintaining linear size of the resulting BP. This is similar to OBDDs however the BPs we target are not ordered, have unbounded degree and arbitrary labeling of edges by input variables. The resulting BPs can be directly realized using new switching devices including Optical Ring Resonators, Ballistic Deflection Transistors and possibly Memristors. The goal is to study an alternative to CMOS gate technology for realizing digital circuits, one that are significantly faster and more power efficient.

Other systems implemented in the past include:

- Source-level merging, a compiler for merging two (and hence more) independent concurrent programs into a single program. The goal is to trade thread-level parallelism by improved scheduling inside the CPU.
- Python Bytecode optimizations. This is a compiler that implements Unrolling, Inlining, and Dataflow optimizations overcoming dynamic aspects of Python.
- A parallel engine for executing DB queries using a cluster of PCs over J2EE.
- The DOL system, a simple compiler that generates boolean gates out of a restricted variant of C.

- ParC compiler and simulator targeting a cluster of PCs using a distributed shared memory (DSM) kernel wherein shared memory is simulated by moving memory pages between the PCs.
- IFAS, a simulator for AD-HOC networks supporting: different types of routing algorithms, highly visualized monitoring, many types of mobile agents and reflections of radio-signals.
- IFS an Internet File system allowing parallel read/write/open/close operations to files while maintaining load-balancing through universal hashing.
- PBD a block device that extends Linux's kernel to support parallel read/write/open/close operations to files by a cluster of Linux machines (updating the hard-disc from "bellow" through remote communication).
- IDOS a peer-to-peer system for ecommerce applications including publish-subscribe and public auctions. The system uses random walks of a set of postmen to complete these transactions.
- A peer-to-peer barter system wherein users enters different combinations of possible barters they would like to exchange. The system, distributively resolve these barter-equations and produce large barter-cycles that maximizes the number of satisfied users.
- HparC an extension of ParC combining message passing and shared memory programming in a uniform manner. HparC was designed to program a cluster of shared memory machines. HparC include a compiler and a run-time system and was used to create an electronic mint over the Internet.

l In Preperation

1. **Y. Ben Asher**, Gil Rapaport and Eyal Zaks *Chorus – C Higher Order Vector Semantics using Whole Function Vectorization*
2. **Y. Ben Asher**, G. Haber, Y. Gendel, Y. Sajrawi and O. Segal, *1K Cores FPGA Shared Memory Architecture for SoC*,
3. **Y. Ben Asher**, G. Haber, and Y. Sajrawi, *A Study of Conflicting Pairs of Compiler Optimizations*,
4. **Y. Ben Asher** and I. Lipov, *Unifying Scheduling with Place and Route for Highlevel Synthesis*,
5. **Y. Ben Asher**, J. Haj-Yihia and A. Yasin *Dynamic Profile Guided Energy Effcient Optimization*,